GLITCHLESS CLOCK SELECTION CIRCUIT

ABSTRACT OF THE DISCLOSURE

A clock selection circuit for selecting between two clock sources. The clock selection circuit has two independent clock inputs, CLK1 and CLK2, where no assumptions are made regarding frequency or phase relationship between the two clocks inputs. Two asynchronous inputs, START1 and START2 (both active high), are used to start and stop the clocks. As long as one clock is active, the START signal of the other clock will not have any effect. The invention includes interlock circuitry that ensures that at any given time only one clock is enabled to the output. Disabling the corresponding START signal disables the clock signal.